IN THE CLAIMS

Claims 1-8 (Canceled)

9. (Currently Amended) A semiconductor integrated circuit device having a plurality of word lines extending in a first direction, a plurality of bit lines extending in a second direction intersecting the first direction, and a plurality of memory cells each including a transistor and a capacitor disposed on the bit lines, said semiconductor integrated circuit device comprising:

active regions formed on a semiconductor substrate, extending in a third direction different from the first and the second directions and each intersecting ~~the~~ two of the word lines and ~~the~~ one of the bit lines;

first and second semiconductor regions formed in the active regions and serving as sources and drains of the transistors;

first and second electrodes for forming the capacitors;

a dielectric film formed between the first and the second electrodes;

a first insulating film formed between the bit lines and the first electrodes; and

a first conducting layer having portions formed in first openings formed in the first insulating film and electrically connecting either of the first and the second semiconductor regions to the first electrodes;

wherein portions of the first conducting layer are arranged in regions surrounded by the word lines and the bit lines, respectively, ~~and~~ the portions of the first conducting layer ~~has~~ have a width in the second direction smaller than that of the word lines, and a center of the portions of the first conducting layer is placed off of a center line of said active regions directed in the third direction.

10. (Currently Amended) The semiconductor integrated circuit device according to claim 9, further comprising a second conducting layer formed between the first conducting layer and either of the first and the second semiconductor regions, wherein a width with respect to the first direction of portions of the second conducting layer is greater than that of the portions of the first conducting layer.

11. (Currently Amended) The semiconductor integrated circuit device according to 10, wherein a center distance with respect to the first direction between ~~the~~ adjacent portions

of the second conducting layer is smaller than that between ~~the~~ adjacent portions of the first conducting layer overlying the second conducting layer.

12. (Currently Amended) The semiconductor integrated circuit device according to claim 10, wherein a center distance with respect to the second direction between ~~the~~ adjacent portions of the second conducting layer is greater than that between ~~the~~ adjacent portions of the first conducting layer overlying the second conducting layer.

13. (Currently Amended) The semiconductor integrated circuit device according to claim 10, wherein a silicon nitride film is formed between the word lines and the second conducting layer, and ~~any~~ no silicon nitride film is ~~not~~ formed between the bit lines and the first conducting layer.

14. (Currently Amended) The semiconductor integrated circuit device according to claim 9, wherein a width of the bit lines is smaller than that of the word lines.

Claims 15-23 (Canceled)